
Vision Series: Power Management

Atmel Corporation

Redefining Low Power in
Cortex-M4 Processor-based MCUs



Presentation Outline

- Introducing SAM4L
- SAM4L design optimization for energy efficiency
 - General Architecture description
 - Clock Management
 - Power Management
 - Flash Controller
- Low Power Techniques
 - Power Saving Modes & Power scaling
 - Peripheral event system & Sleep Walking integrated
- Application Specific Peripherals
- Ecosystem
 - Atmel Studio / ASF
 - SAM-BA

What do you need for your next low power project?

- Energy Efficiency
 - Reduced power consumption
 - Extended battery life
 - Fast wake-up
- Uncompromised Performance and Functionality
 - Powerful CPU
 - User interface capabilities
- Cost Efficiency
 - High integration
 - Reduced BOM cost
- Ease of Use



Bringing picoPower Technology to the ARM Platform

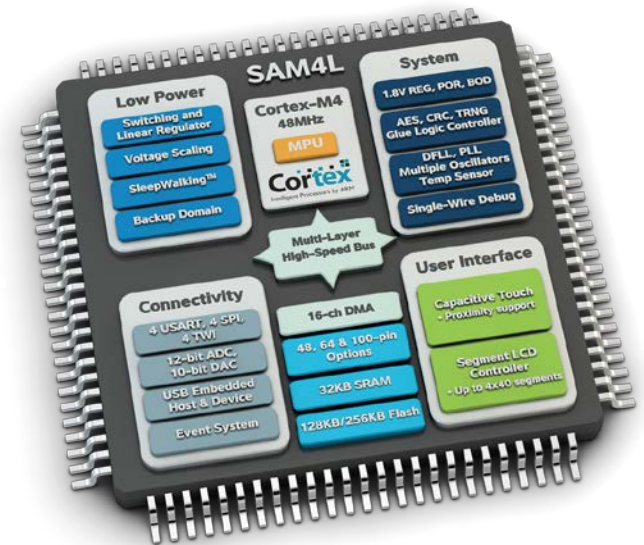
- Continuous Power Saving Innovation
- Designed from the ground up for lowest possible power consumption
- Innovative Device Features and low power techniques



Run Mode	UC3B (2007)	UC3L (2010)	SAM4L (2012)
Active	308 μ A/MHz	165 μ A/MHz	95 μ A/MHz
Full RAM retention	15 μ A	7 μ A	1.5 μ A
Backup	25 μ A	0.9 μ A	0.9 μ A

The World's most power efficient Cortex-M4

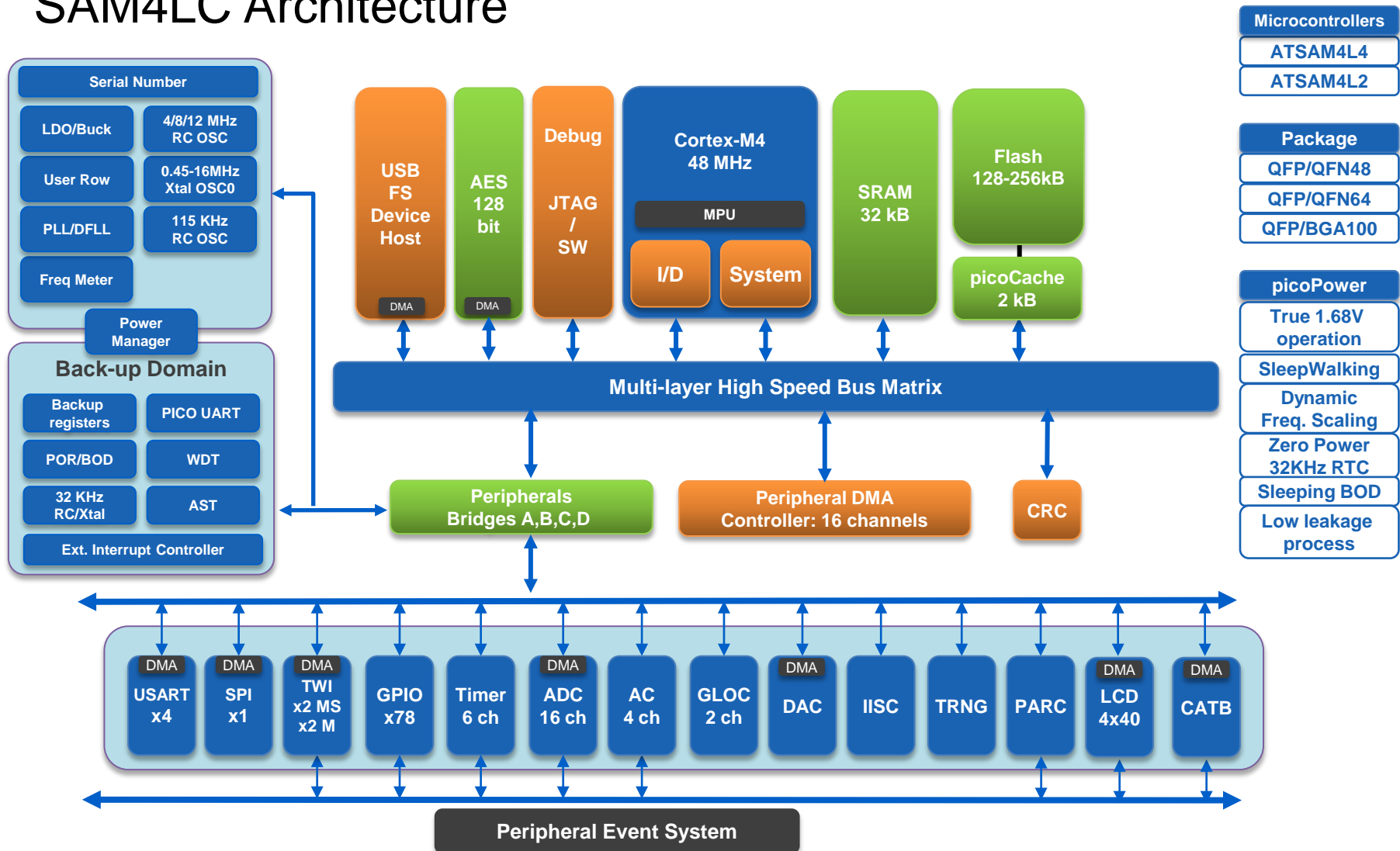
- Optimized for Low-Power Applications
 - Industry's lowest power consumption
 - Active mode: down to 95µA/MHz
 - RAM retention mode : 1.5µA
 - 1.8 – 3.6V operation
 - No degraded performance (up to 48 MHz)
 - Fast wakeup
 - 1.5µs
- Integrated Hardware QTouch®
 - Wake up from deep sleep with a touch of a button or proximity
- Integrated LCD controller
 - 4x40 Segment LCD



SAM4L Family Overview: two series for maximum flexibility

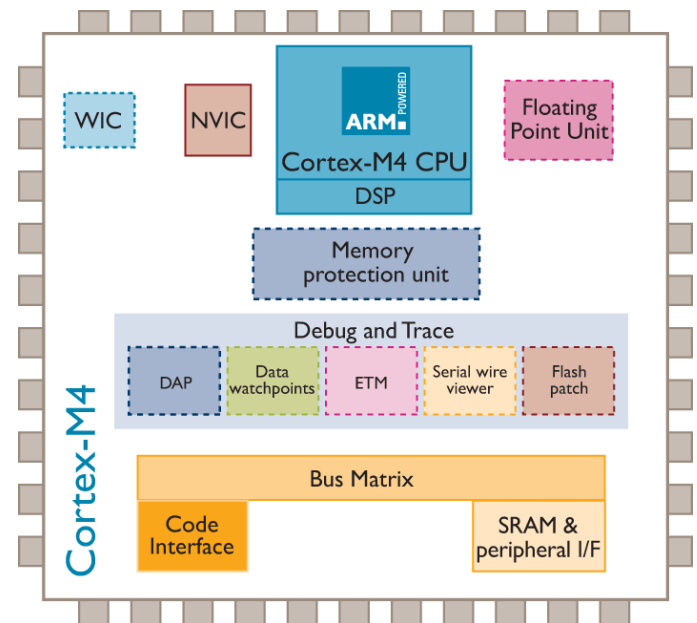
	SAM4LC Series			SAM4LS Series		
Pins	100	64	48	100	64	48
LCD	4x40	4x23	4x13	No	No	No
Hardware Crypto	Yes	Yes	Yes	No	No	No
USB	Host and Device	Host and Device	Host and Device	Device	Device	Device
GPIO	75	43	27	80	48	32
256KB Flash	SAM4LC4C	SAM4LC4B	SAM4LC4A	SAM4LS4C	SAM4LS4B	SAM4LS4A
128KB Flash	SAM4LC2C	SAM4LC2B	SAM4LC2A	SAM4LS2C	SAM4LS2B	SAM4LS2A
I ² C	2 Master + 2 Master/Slave	2 Master/Slave	1 Master/Slave	2 Master + 2 Master/Slave	2 Master/Slave	1 Master/Slave

SAM4LC Architecture



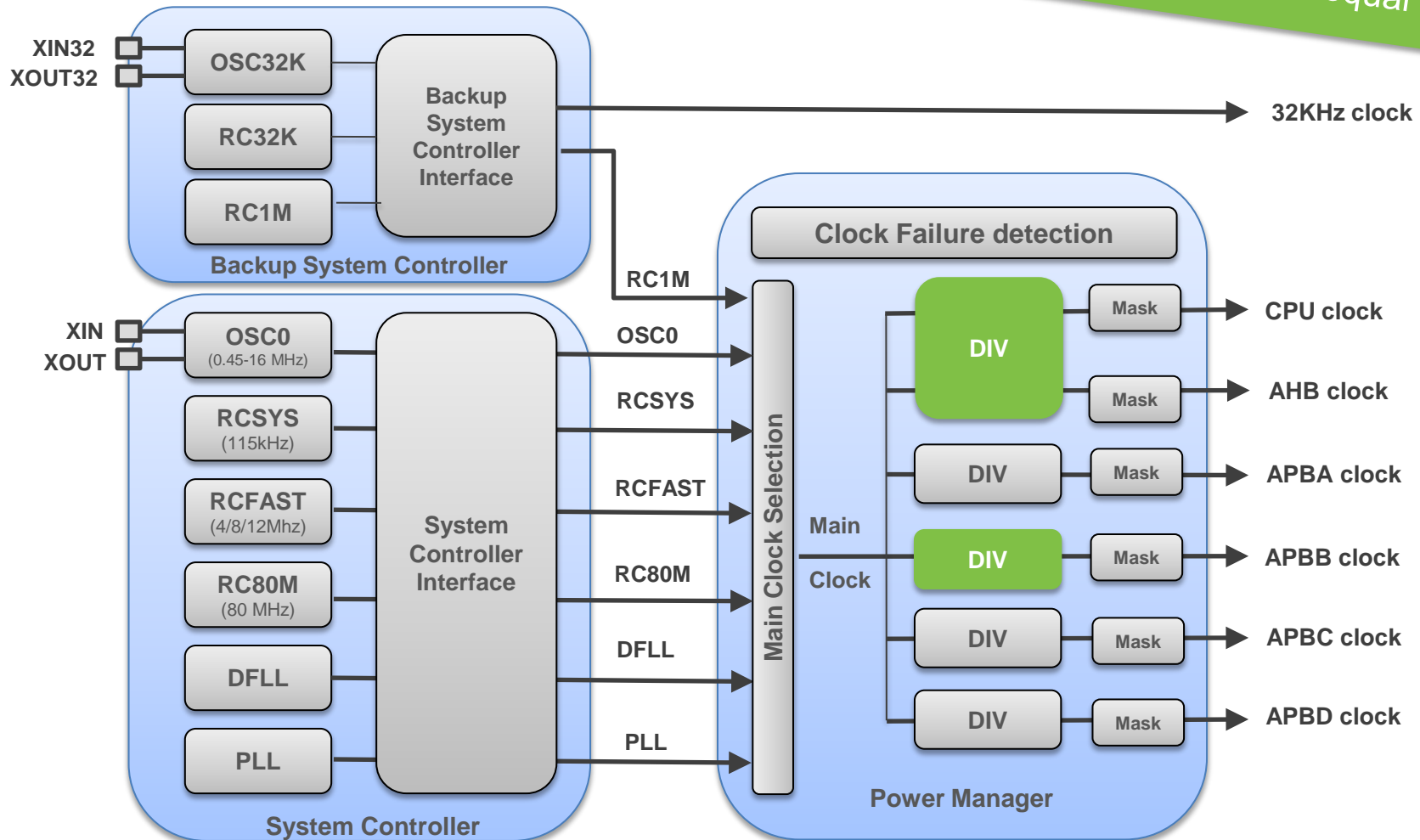
Cortex-M4 core enables highly efficient signal processing

- Cortex-M4 frees CPU resources in case digital signal processing task are used (less active cycles are needed)
- Features:
 - ARMv7ME Architecture Thumb-2 Technology
 - Compatible with Cortex-M3
 - DSP and SIMD extensions
 - Low power modes
 - Interrupt Controller (NVIC)
 - Optional Memory Protect Unit (MPU)



SAM4L Flexible Clock Management

CPU, AHB and APBB
clocks must be equal



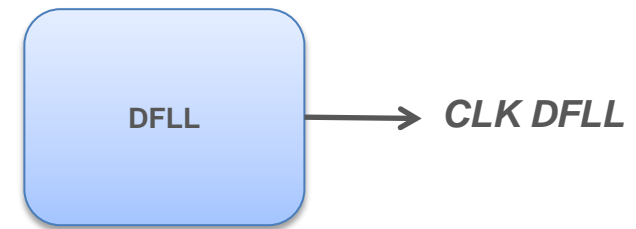
SAM4L Clock Mask System

Bit	CPUMASK	HSBMASK	PBAMASK	PBBMASK	PBCMASK	PBDMASK
0	OCD	PDCA	IISC	FLASHCALW	PM	BPM
1	-	FLASHCALW	SPI	HRAMC1	CHIPID	BSCIF
2	-	HRAMC1 (PicoCache RAM)	TC0	HMATRIX	SCIF	AST
3	-	USBC	TC1	PDCA	FREQM	WDT
4	-	CRCCU	TWIM0	CRCCU	GPIO	EIC
5	-	APBA bridge	TWIS0	USBC		PICOUART
6	-	APBB bridge	TWIM1	PEVC		
7	-	APBC bridge	TWIS1			
8	-	APBD bridge	USART0			
9	-	AESA	USART1			
10	-				

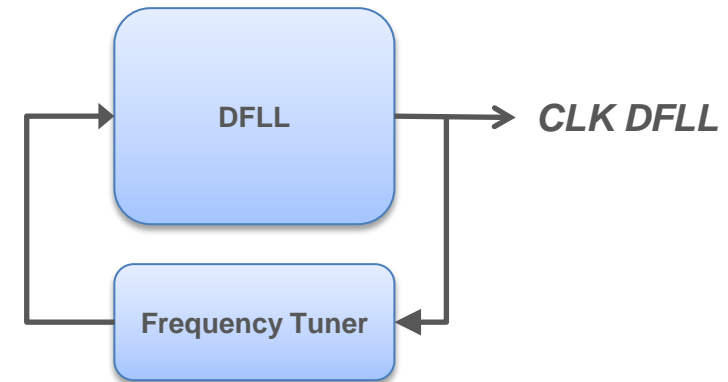
* Peripheral clocks in black are enabled by default after reset

Digital Frequency Locked Loop (DFLL)

- Can be used as :
 - Programmable oscillator (open loop)
 - Accurate frequency multiplier (closed loop with frequency Tuner)
- Can generate 20 – 220MHz output
- Additional spread spectrum option
 - Provides better EMC
- Advantages vs. PLL :
 - No external components required
 - Can run from 32KHz sources
- Constraints vs. PLL :
 - Lower accuracy (0,5% drift error max) preventing USB use

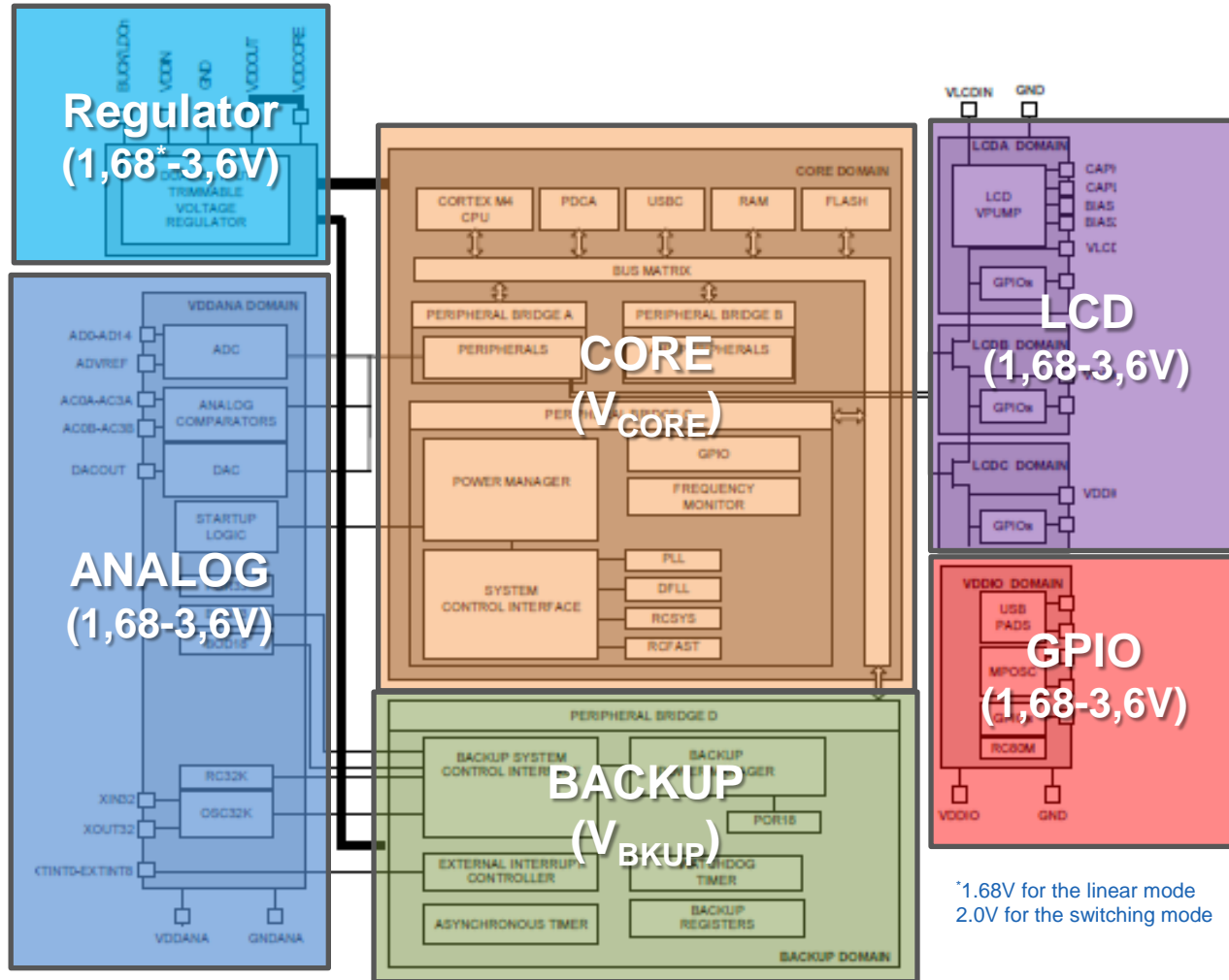


Programmable oscillator mode



Accurate frequency multiplier mode

SAM4L Power Domains



- Enables single 1.68V-3.6V Power Supply
- Outputs voltage in Core (VCORE) and Backup (VBKUP) domains:
 - VBKUP remains always powered
 - VCORE not powered in backup mode only

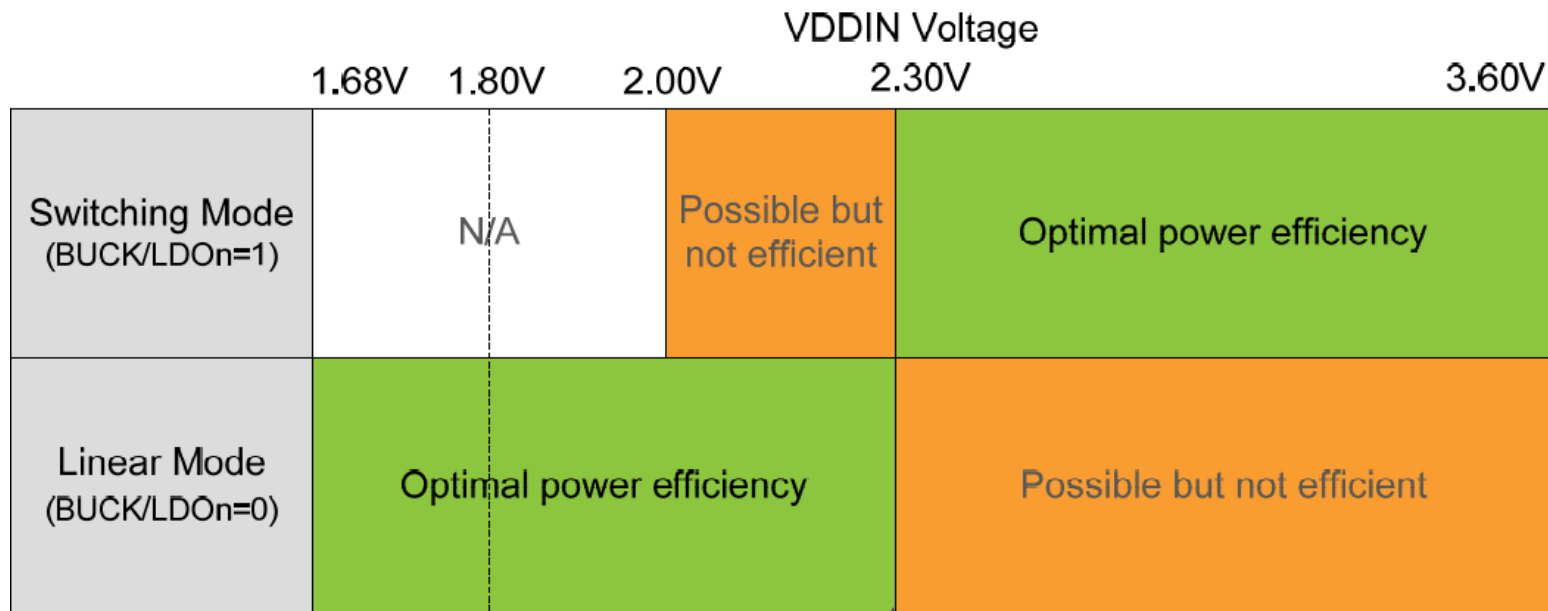


Voltage regulator functional modes

- SAM4L voltage regulator has two functional modes:
 - Switching mode (BUCK)
 - Linear mode (LDO)
- Modes selection using BUCK/LDO pin:
 - Sampled once at POR
 - Then available as a GPIO (PA02)

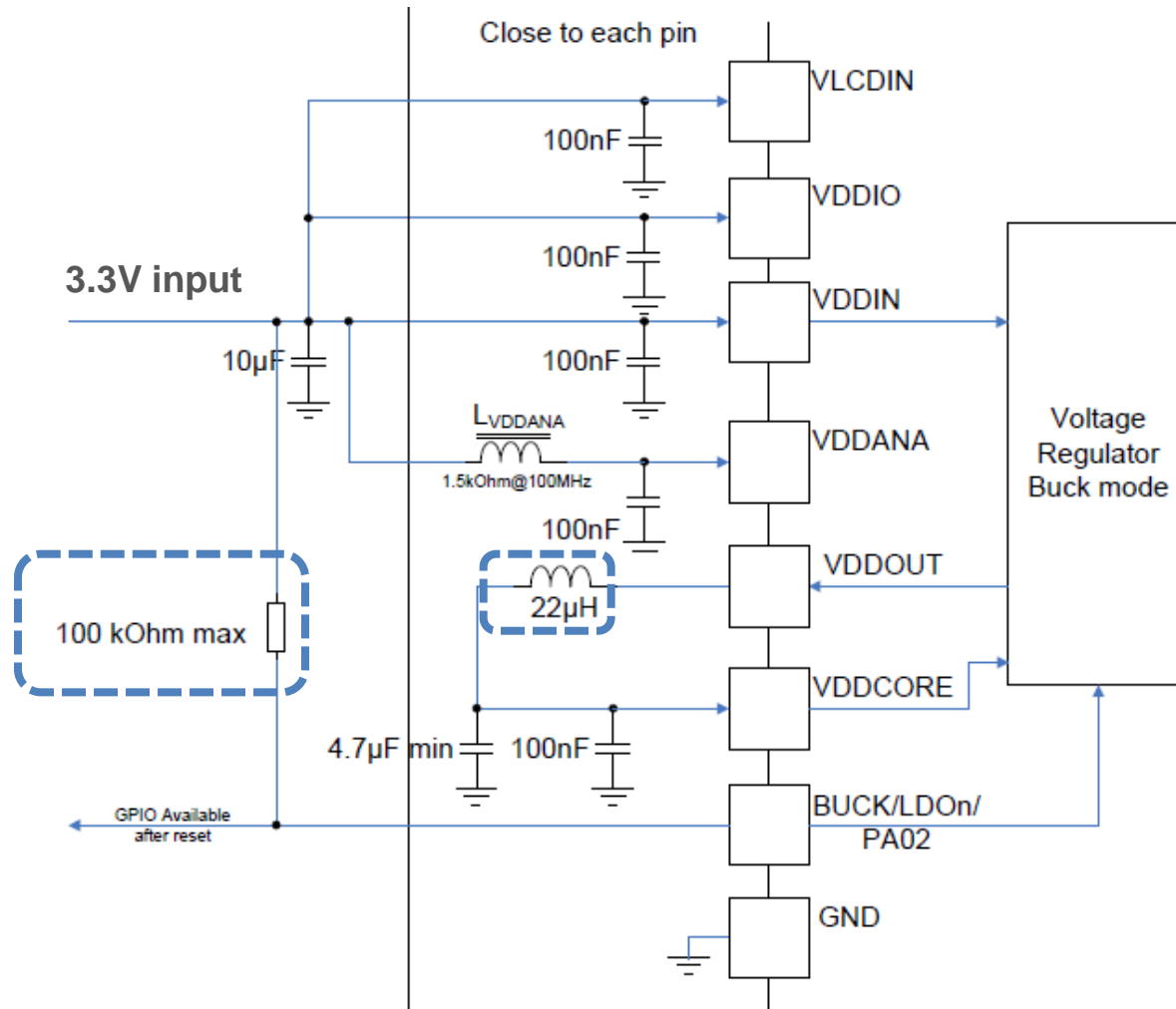
Choosing the right regulator mode for the application

- Voltage regulator choice depends on VDDIN:

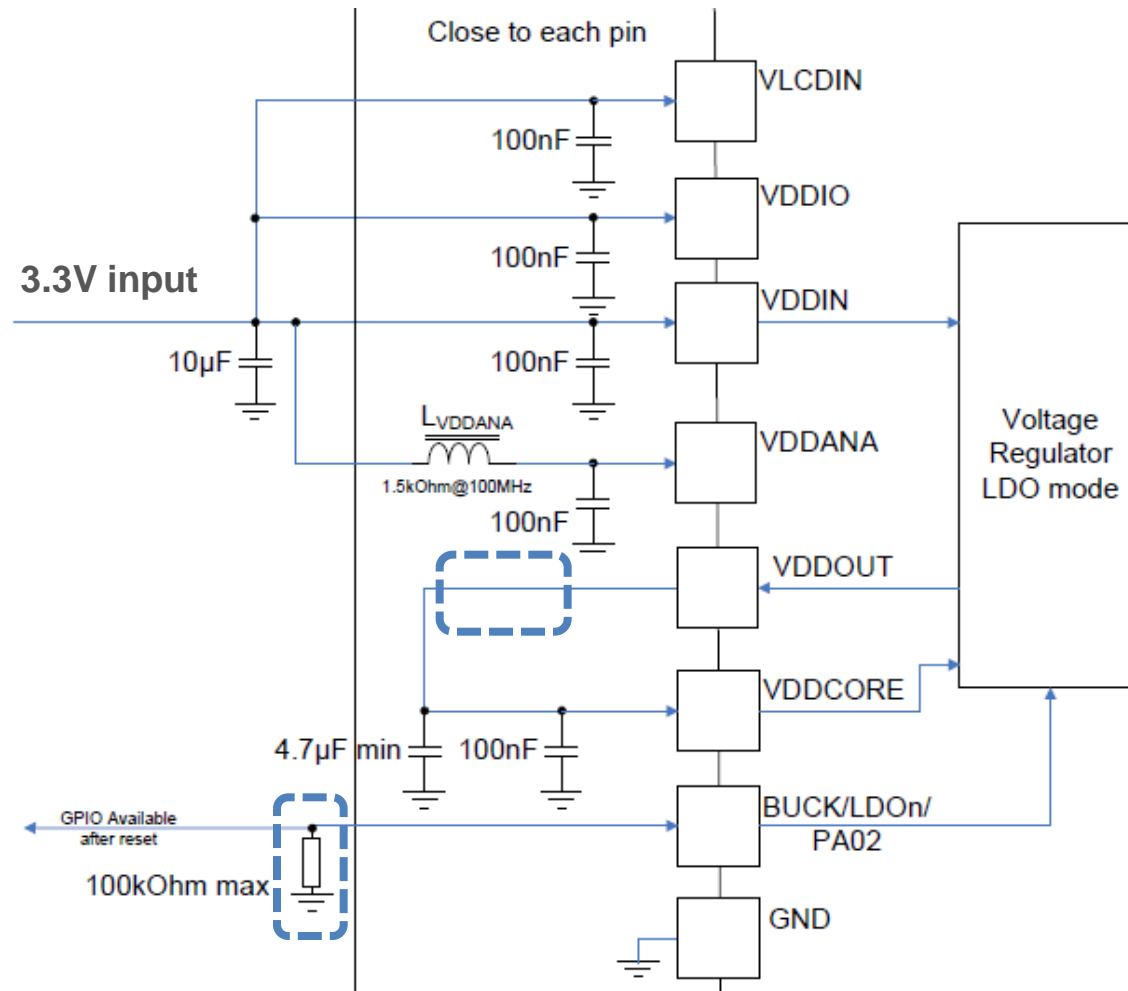


Below 2.3V, linear mode is more power efficient than switching mode.

Power supply strategy: Switching mode



Power supply strategy: Linear mode



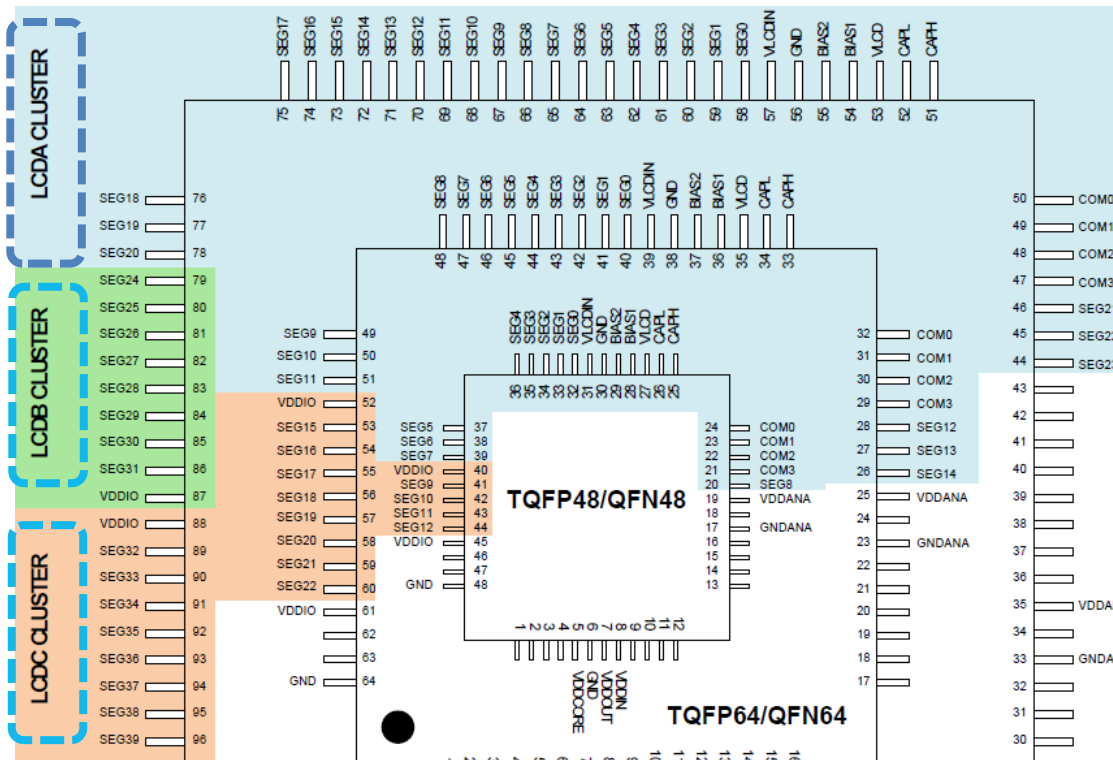
Regulator modes Pros & Cons:

Criteria	Switching Mode	Linear Mode
Power Efficiency	Optimal when $V_{DDIN} > 2,3V$	Optimal when $V_{DDIN} < 2,3V$
Consumption ($V_{DDIN} = 3,3V$; $F_{CPU} = 12MHz$)	95uA/MHz	208uA/MHz
BOM cost	Requires an external 22uH inductor. Requires a good quality ceramic capacitor on VDDCORE.	No extra component
Emitted noise	Proper filtering and decoupling is needed in noise sensitive applications.	Fits for noise sensitive applications

trade-off between low power, BOM cost (external components required in switching mode) and noise sensitivity

SAM4LC Segment LCD Power Modes

- Three clusters (A, B, C) powered independently

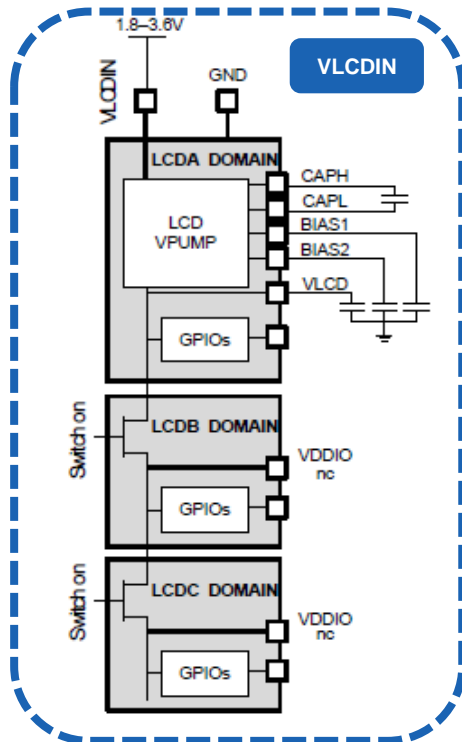


- For each cluster, LCD pads can either be in GPIO or LCD mode

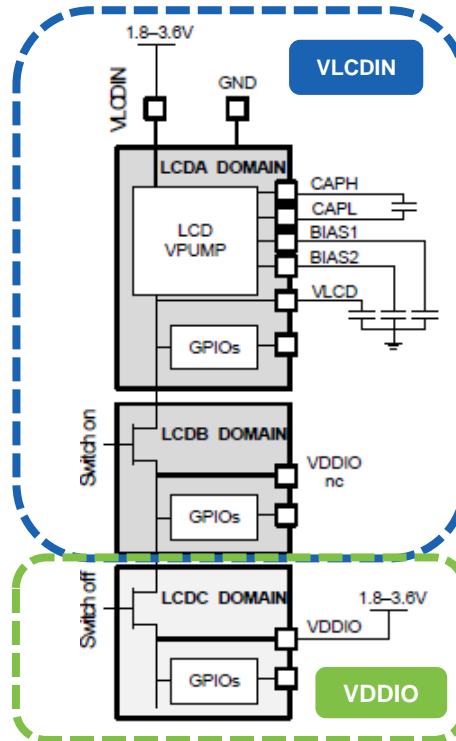
SAM4LC Clusters configurations

- 100-pin package example

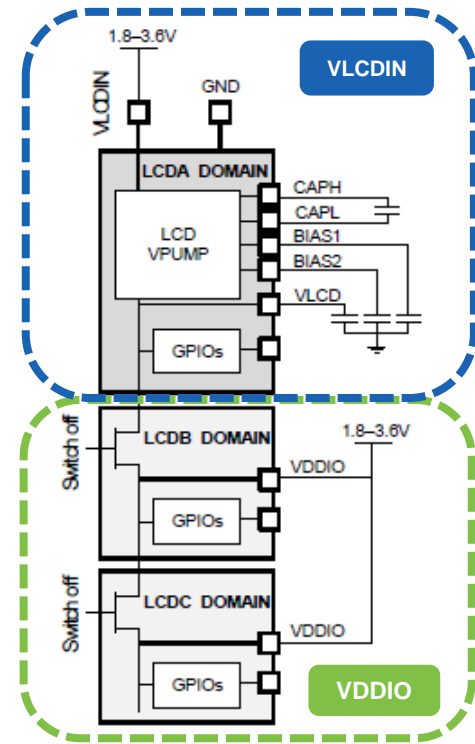
Up to 4x40 segments
No GPIO in LCD clusters



Up to 4x32 segments
Up to 8 GPIOs in LCDC clusters

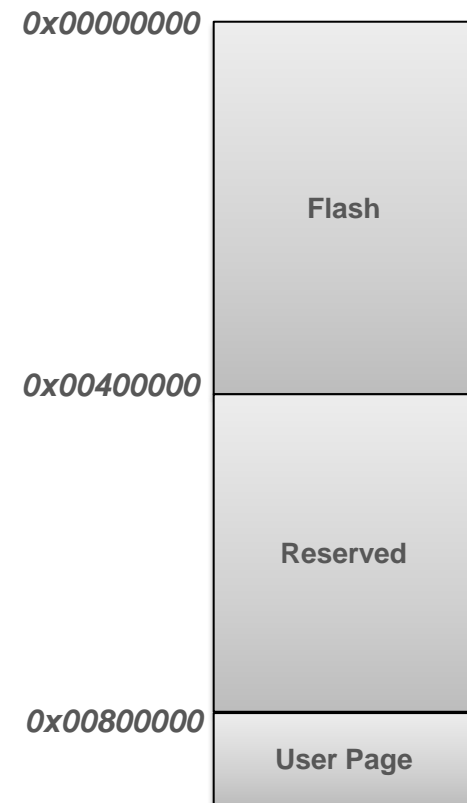


Up to 4x24 segments
Up to 16 GPIOs in LCDB & LCDC clusters



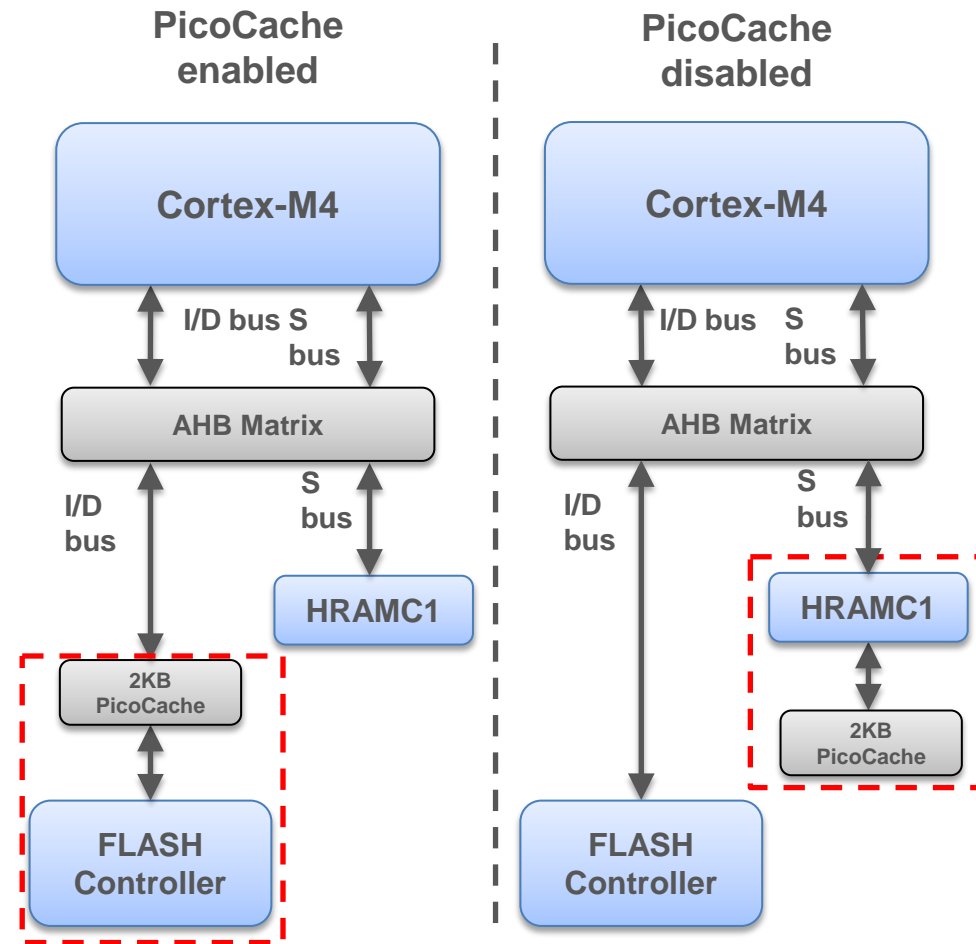
Flash and Flash Controller

- Flash characteristics :
 - Single plane 128 or 256KB
 - 64-bit wide access
 - 0 wait state up to 24 MHz
 - 1 wait state up to 48 MHz
- Flash Controller :
 - User Page for device specific configuration
 - 16 lockable regions of equal size
 - Security bit to lock device from Debug access
 - PicoCache enabling/disabling



picoCache to minimize flash active power & improve performances

- Tightly coupled to the Flash memory for better efficiency
 - Compensate wait state penalty
- Decreasing device power consumption between 10% to 15% range.
- Not suitable if
 - 0 Wait State
 - Deterministic tasks to be executed
- Can be used as a supplementary system RAM when disabled.



The Backup Power Manager

- The Backup Power Manager (BPM) implements different solutions to reduce the power consumption
 - 4 Power Save modes : intended to reduce the logic activity depending on application needs.
 - Sleep mode
 - Wait mode
 - Retention mode
 - Backup mode

Select mode entry by SLEEPDEEP , BKP and RET bit combination

- Power Scaling : intended to scale the power configuration

Power Save Modes: Sleep Mode

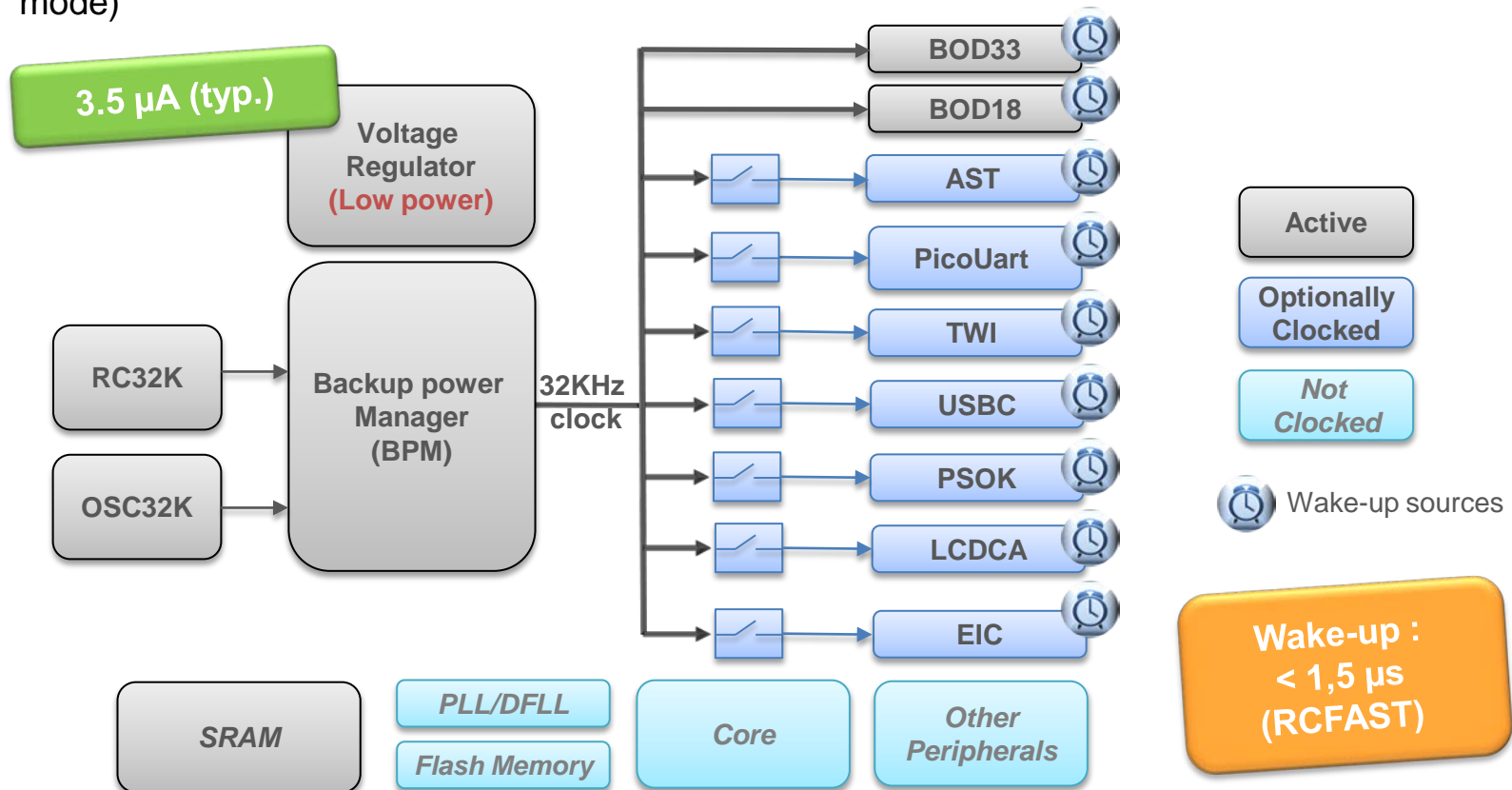
- Entry Mode : WFI , SLEEPDEEP = 0 , BKP = 0 , RET = 0
- Allows first level power optimization with the fastest wakeup time
- 4 available Sleep modes for better clock flexibility

Mode	CPU clock	AHB clocks	APB clocks	Clock sources : OSC,RCFAST,RC80M, PLL , DFLL	RCSYS	OSC32 RC32K	Wake up sources	Consumption min
0	Stop	Run	Run	Run	Run	Run	Any interrupt	527uA
1	Stop	Stop	Run	Run	Run	Run	Any interrupt	369uA
2	Stop	Stop	Stop	Run	Run	Run	Any interrupt	305uA
3	Stop	Stop	Stop	Stop	Run	Run	Any interrupt	46 uA

- Additional SLEEPONEXIT mode.

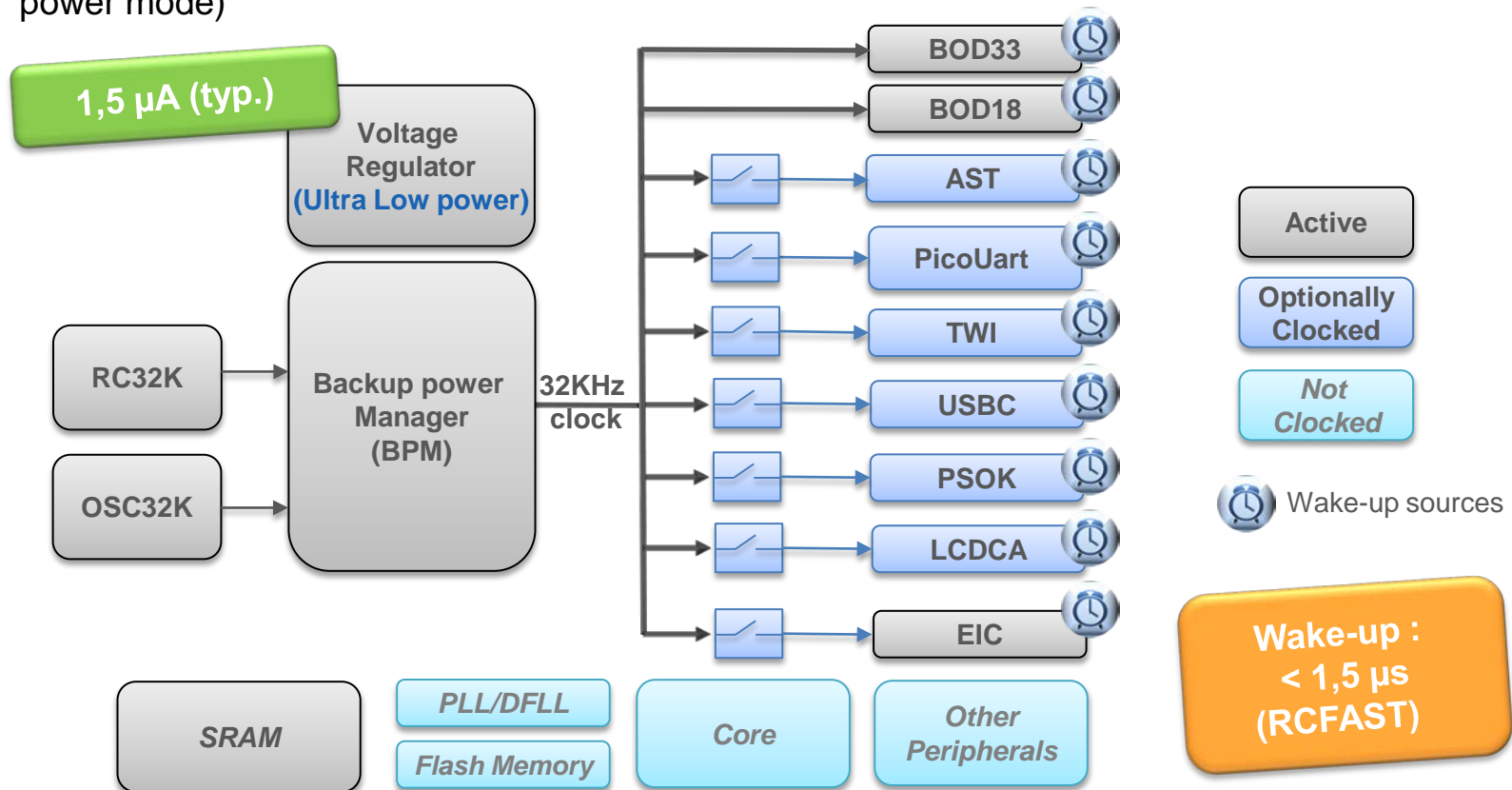
Power Save Modes: Wait Mode

- Entry Mode : WFI , SLEEPDEEP = 1 , BKP = 0 , RET = 0
- All clocks are OFF except 32KHz clock
- Very low power mode with SRAM retention and Sleepwalking (Voltage regulator in low power mode)



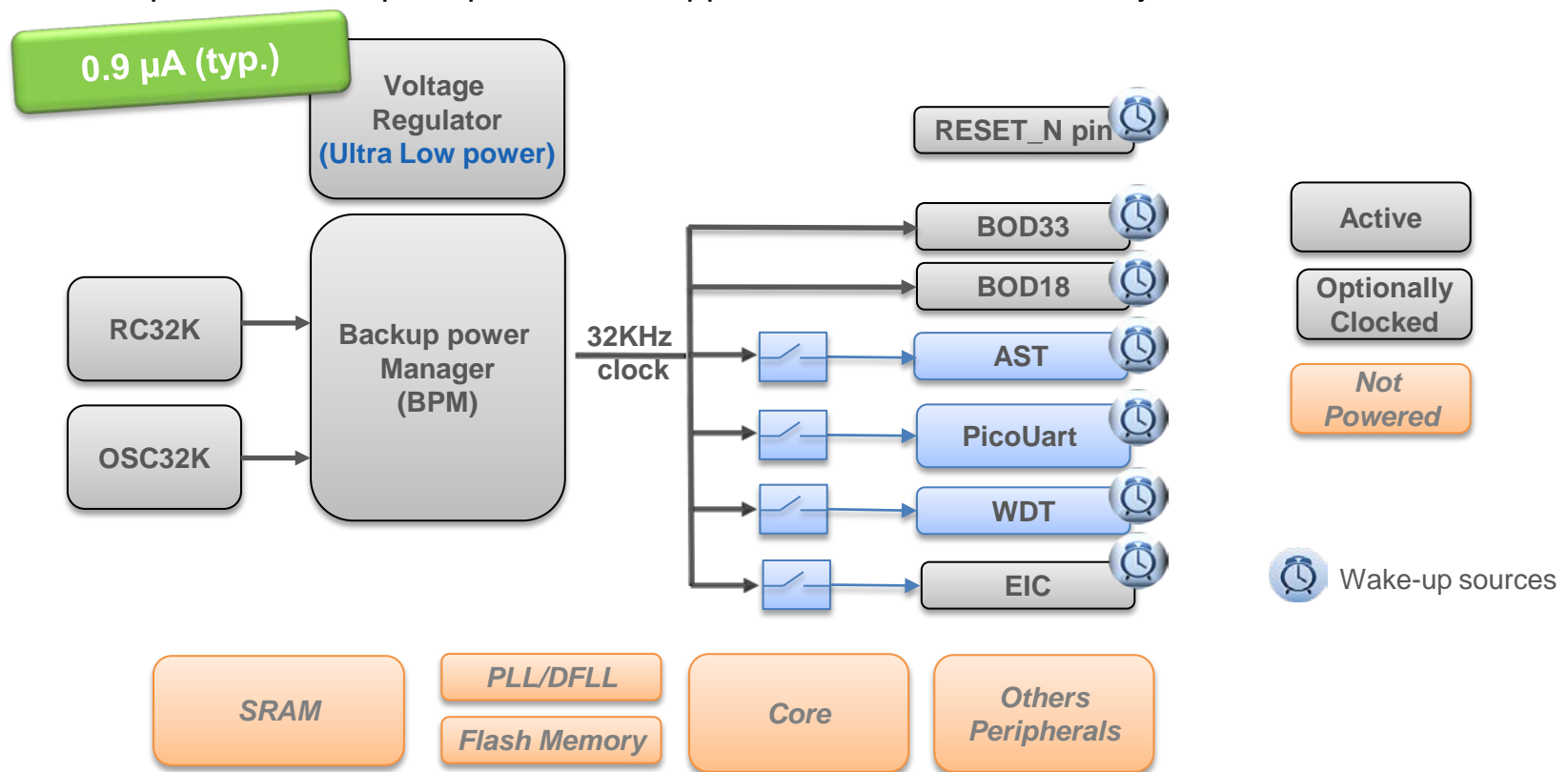
Power Save Modes: Retention Mode

- Entry Mode : WFI , SLEEPDEEP = 1 , BKP = 0 , RET = 1
- All clocks are OFF except 32KHz clock
- Lowest power mode with SRAM retention, Sleepwalking disable (Voltage regulator in ultra low power mode)



Power Save Modes: Backup Mode

- Entry Mode : WFI , SLEEPDEEP = 1 , BKP = 1
- All clocks are OFF except 32KHz clock
- Lowest power consumption possible but application restart is necessary

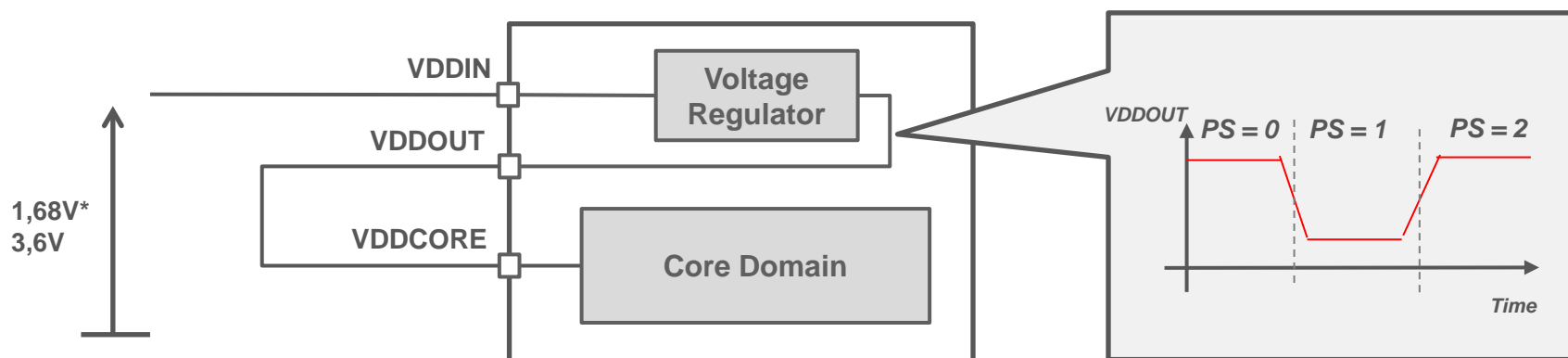


Power Save Modes Summary

Mode	Mode Entry	Wake up sources	Core domain	Backup domain	Consumption Min
RUN	N/A	N/A	CPU clock ON	Selectable clocks are ON.	95 uA/MHz
SLEEP	WFI SLEEPDEEP = 0 BKUP = 0	Any Interrupt	CPU clock OFF Selectable clocks are ON	Selectable clocks are ON.	46 uA
WAIT	WFI SLEEPDEEP = 1 RET = 0 BKUP = 0	PM WAKE interrupt	All clocks are OFF Core domain is retained	All clocks are OFF except RC32K or OSC32K if running	3.5 uA
RETENTION	WFI SLEEPDEEP = 1 RET = 1 BKUP = 0	PM WAKE interrupt	All clocks are OFF Core domain is retained	All clocks are OFF except RC32K or OSC32K if running	1.5 uA
BACKUP	WFI SLEEPDEEP = 1 BKUP = 1	- Ext. Interrupt - BOD33, BOD18 interrupt and reset -AST alarm, periodic overflow. -WDT interrupt and reset external reset on RESET_N Pin.	OFF (not powered)	All clocks are OFF except RC32K or OSC32K if Running	0.9 uA

Power Scaling

- Adjusts the internal regulator output voltage according to application frequency (voltage scaling).

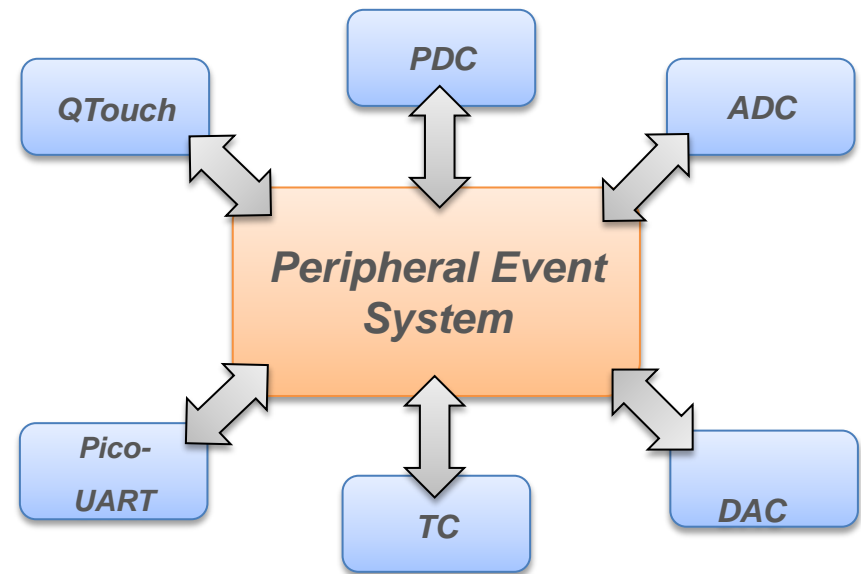


Power Scaling (PS)	VDDIN	Core Frequency	IDDIN Fibonacci algo
0	3.3V	12MHz to 32MHz	177 uA/MHz
1	3.3V	<12MHz	95 uA/MHz
2	3.3V	>32MHz	177 uA/MHz

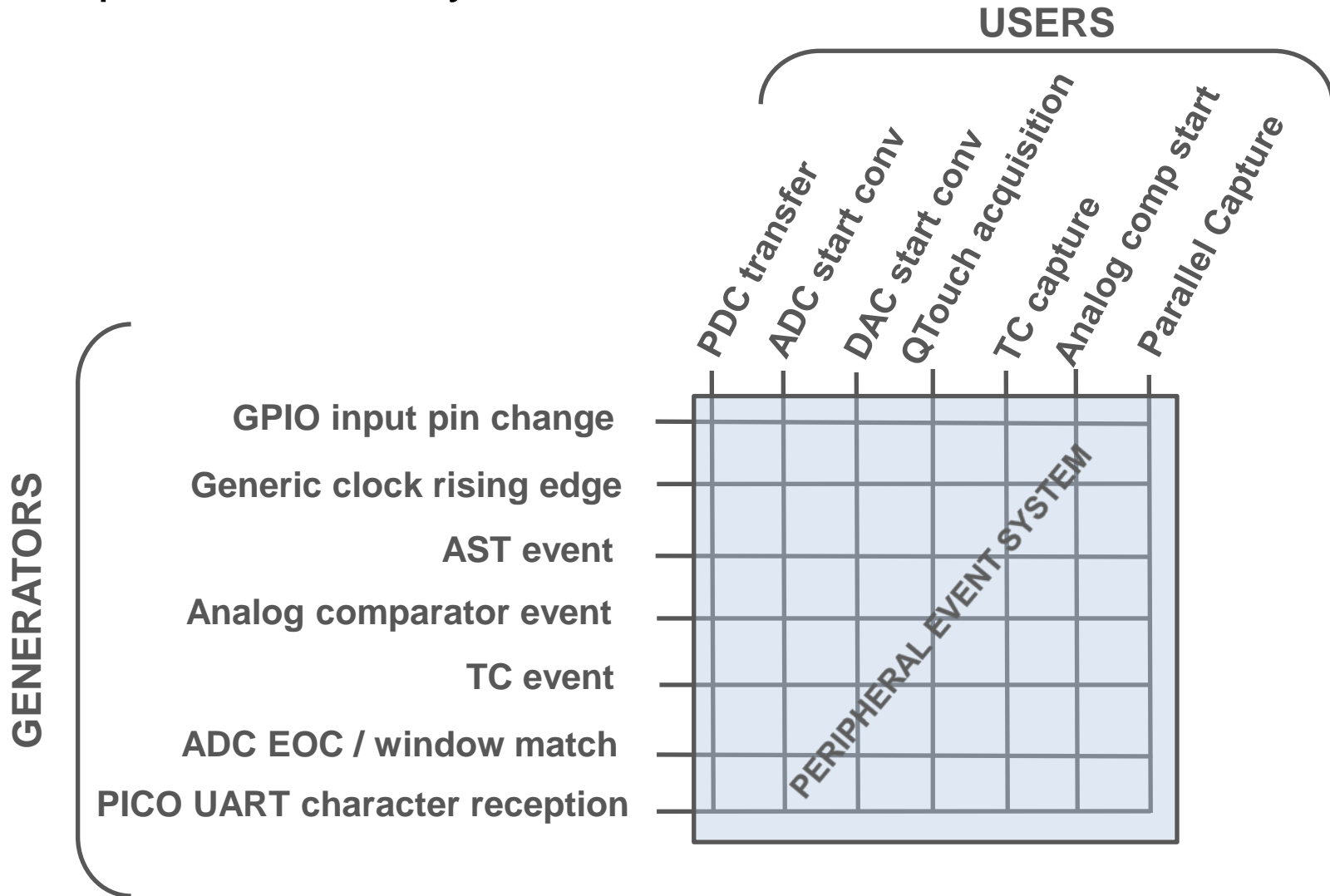
48%

Peripheral Event System

- Inter-peripheral communication
 - CPU and DMA independent
- Latency free event handling
 - Safe fault protection
 - 100% predictable reaction time
- Advantages
 - Precise timing
 - Reduced CPU overhead
 - Reduce Power Consumption

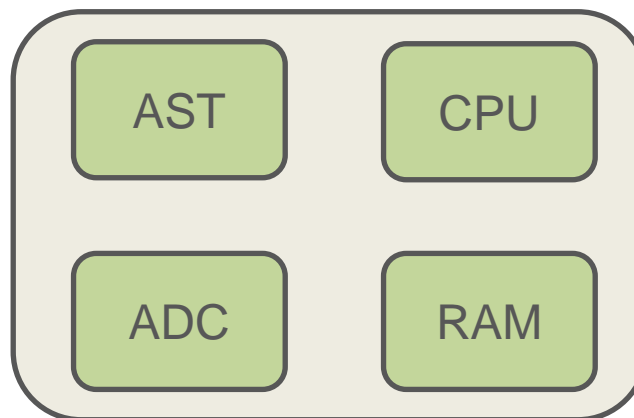


Peripheral Event System Matrix



Sleep Walking

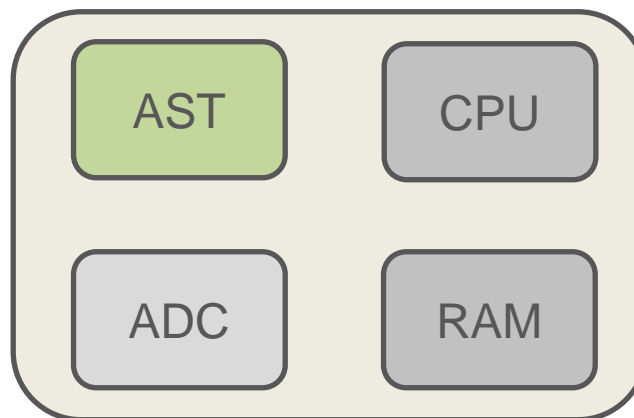
- Intelligent peripherals
 - Compare input value to preset threshold
 - Alert CPU only when threshold exceeded
- Eliminate CPU interrupts
 - Reduce CPU overhead
 - Reduce power consumption in sleep modes
- Temperature monitoring example



Run mode

Sleep Walking

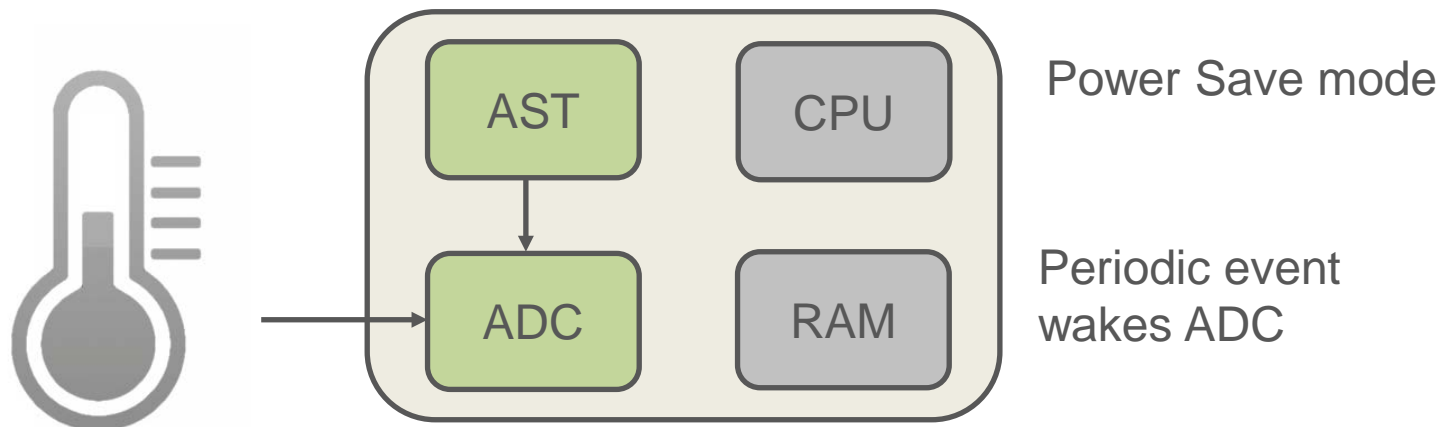
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Power Save mode

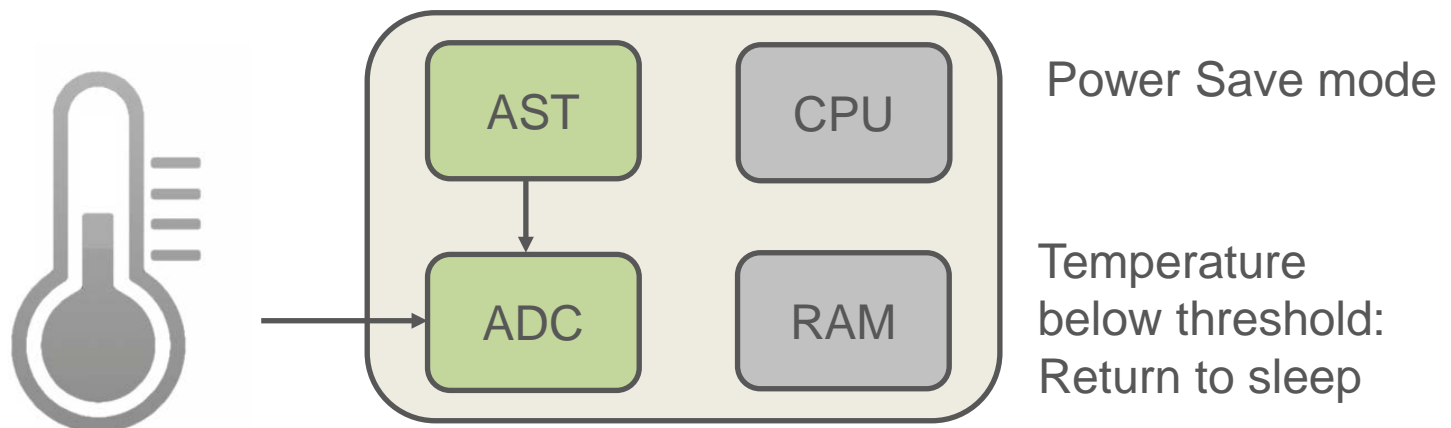
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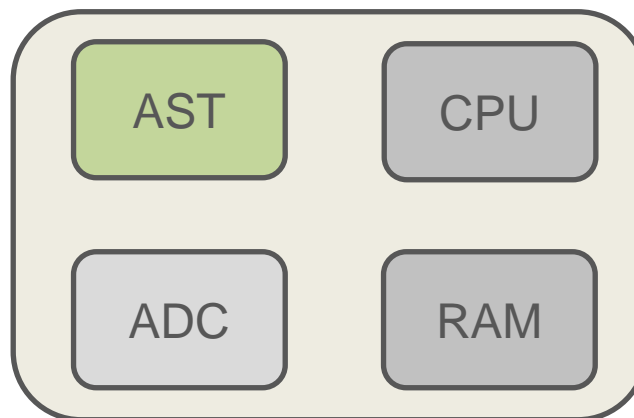
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Sleep Walking

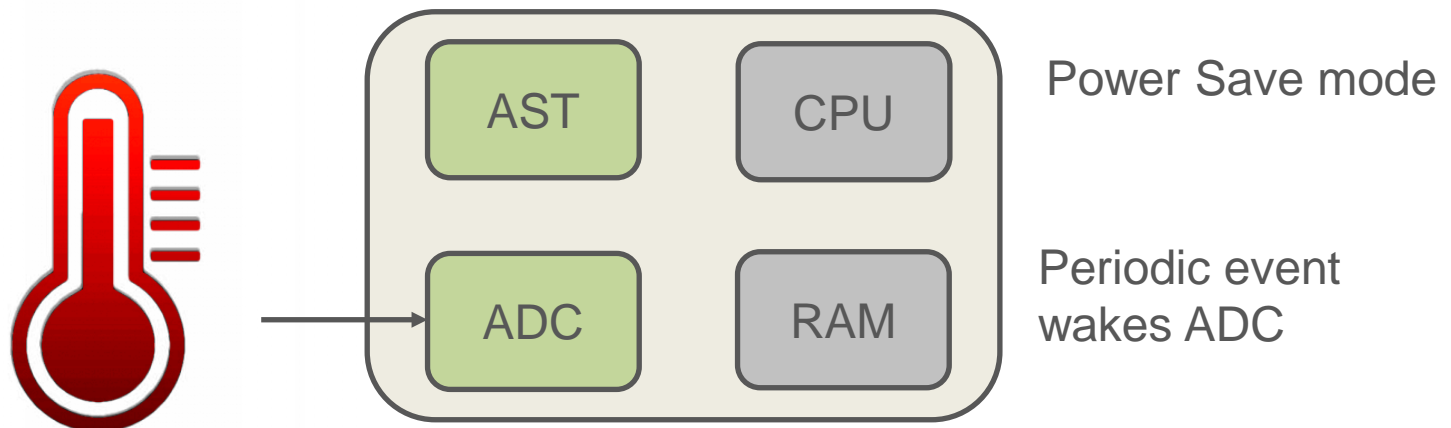
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Power Save mode

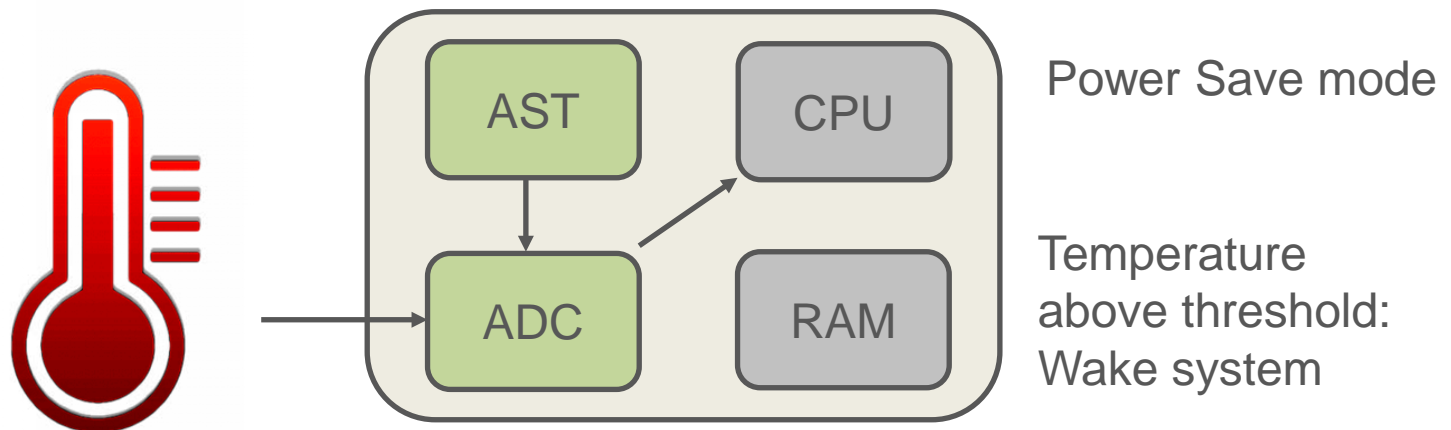
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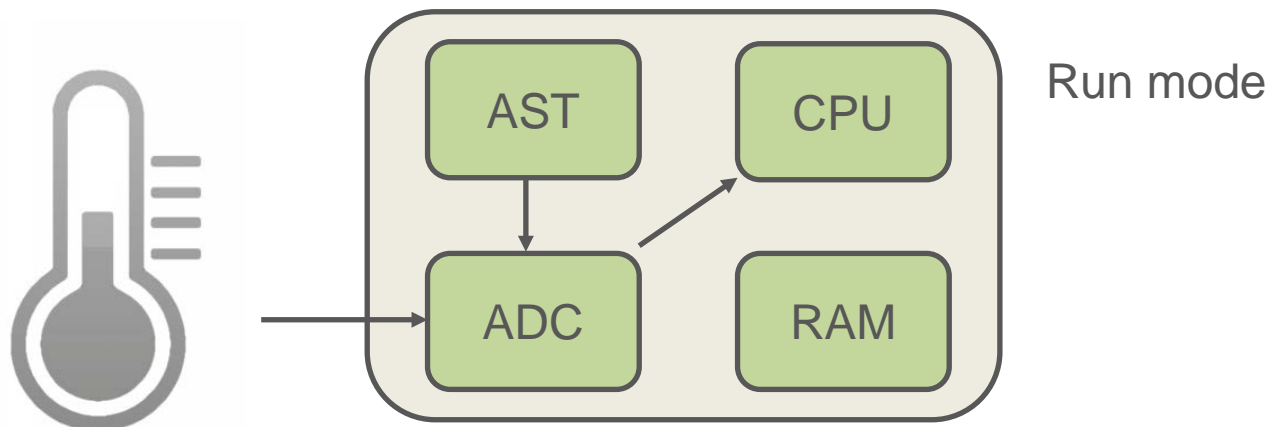
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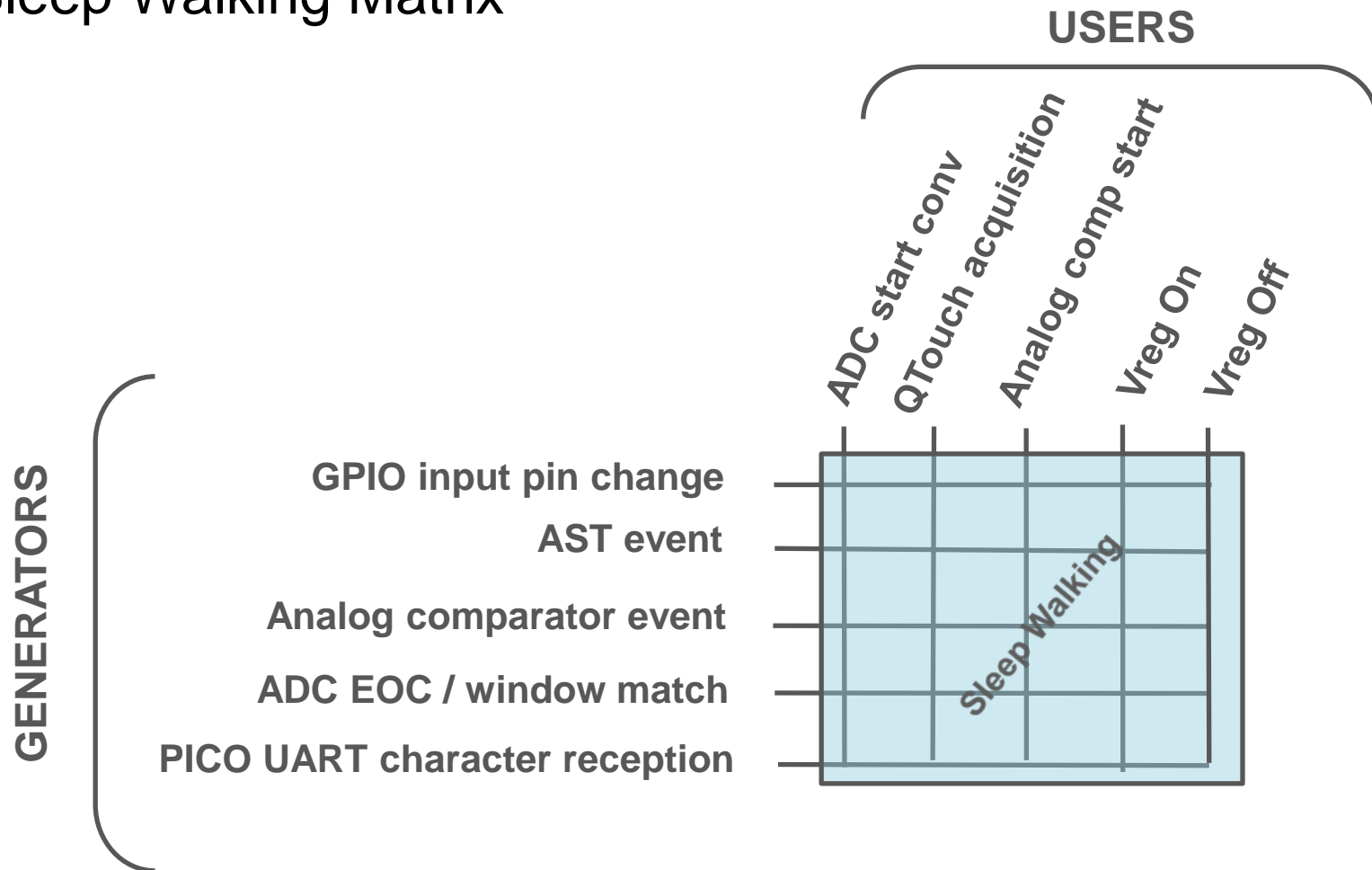


Sleep Walking

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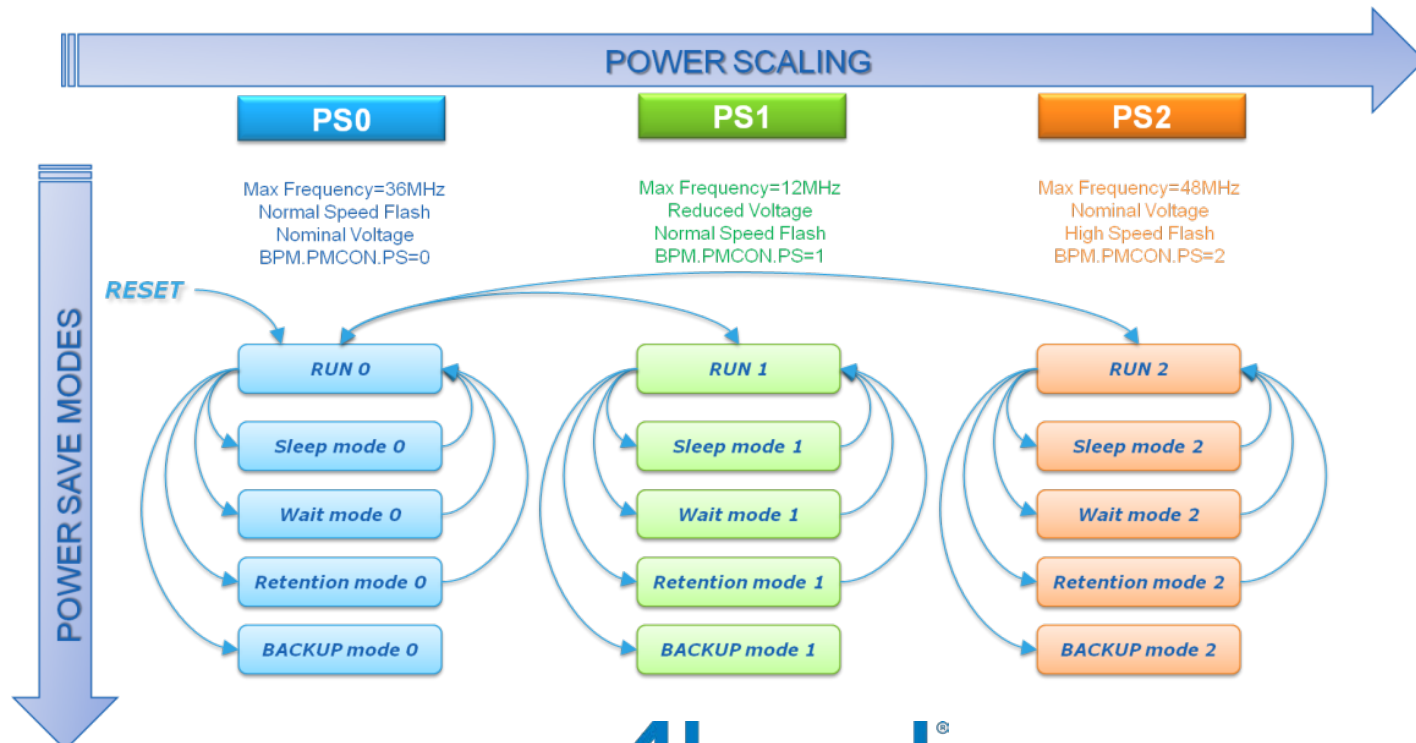


Sleep Walking Matrix



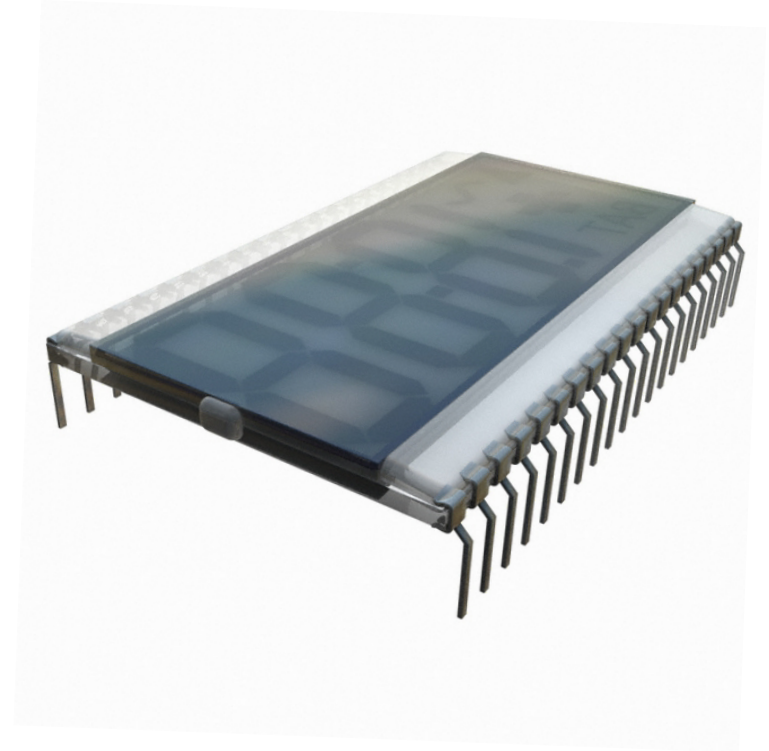
Combining Low Power Design Techniques

- In RUN mode, Power Scaling setting can be adjusted on the fly.
- Power Scaling and Power Save modes can be combined together to reach the lowest consumption according to application performance requirement.



SAM4L LCD Controller (1/4)

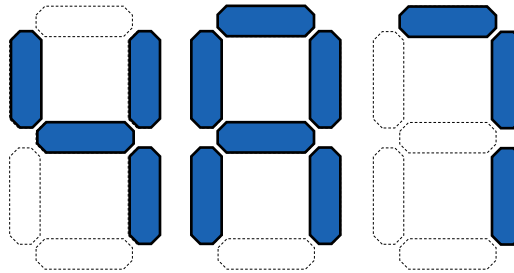
- Up to 4x40 segments
- ASCII character mapping
- Segment blink and display blank
- SWAP mode for flexible board layout



SAM4L LCD Controller (2/4)

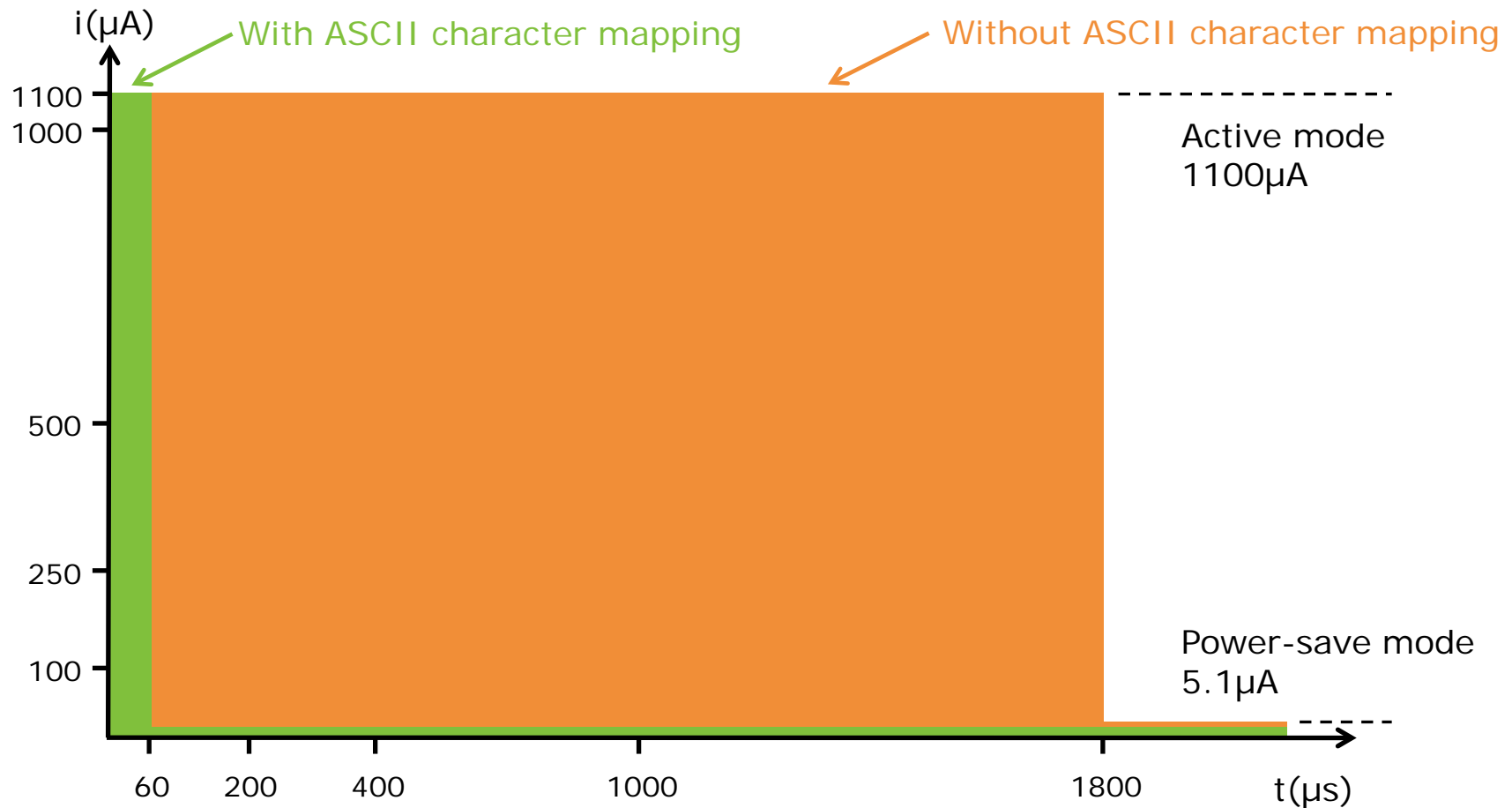
- ASCII Character Mapping
 - Reduce and simplify the software code
 - Decrease the display updating time
 - Reduce power consumption
 - Code example:

```
LCD.CTRLG |= LCD_DIGIT_TYPE | MY_START_SEG_NUMBER;  
LCD.CTRLH = '4';  
LCD.CTRLH = 'A';  
LCD.CTRLH = '7';
```



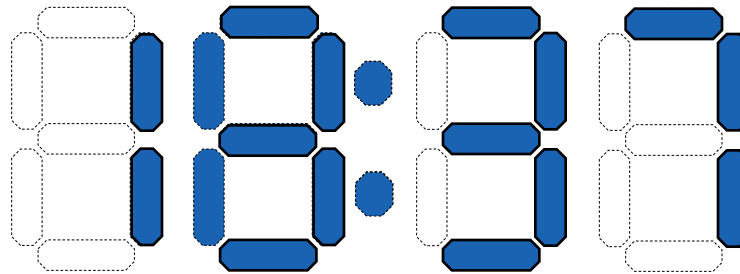
SAM4L LCD Controller (3/4)

- Writing seven 16-segment digits, then enter in power save mode:



SAM4L LCD Controller (4/4)

- Segment Blink
 - Available in Sleep and Active mode
 - Selectable blink frequency
 - Reduce interrupt frequency
 - Reduce power consumption



Capacitive Touch Module

- Low-power and high performance capacitive touch module
 - Touch filtering without CPU intervention
- Endless Configurations (up to 32 sensors)
 - Buttons
 - Sliders
 - Wheels
- Differential or single-ended sensing operation
- Event Driven
 - Touch
 - Out-of-touch
 - Autonomous interrupts
- Peripheral Event System Integration
 - SleepWalking



High-Speed Communication and Analog

- TWI

- I2C compliant
- Master
- Slave
- Transfer speeds up to 3.4 Mbit/s
- 7-bit, 10-bit and General Call addressing
- SMBus Compatible
- Hardware Packet Error Checking



- USB – 12Mbit/s

- Embedded Host
 - Up to 8 endpoints
 - Data buffers in RAM
 - Ping-pong mode
- On-chip transceivers



- 12-bit ADC – 300ksps

- Programmable gain
- Programmable sample & hold

- 10-bit DAC – 500ksps

- DMA support
- Event system integration

Security and Flexibility

- 128-bit AES
 - FIPS197-compliant
 - DMA interface
 - Hardware security measures
- 32-bit True Random Generator
 - NIST 800-22 passed
- Hardware CRC & serial number
- USART
 - Asynchronous and synchronous
 - RS232, SPI, IrDA, RS422, RS485
- PicoUART
 - extended UART wake-up capabilities in all sleep modes
- Parallel Capture (PARC)
 - 8-bit parallel capture
 - DMA and event system support
- Glue Logic Controller (GLOC)
 - Programmable lookup tables
 - Four inputs → one output



Atmel Studio 6 / Atmel Software Framework

- Atmel Studio 6
 - Free, Professional IDE
 - 300 Atmel ARM and AVR MCUs
- Atmel Software Framework
 - More than 1500 Project Examples
 - SAM4L support added in ASF-3.4.1

Learn more:

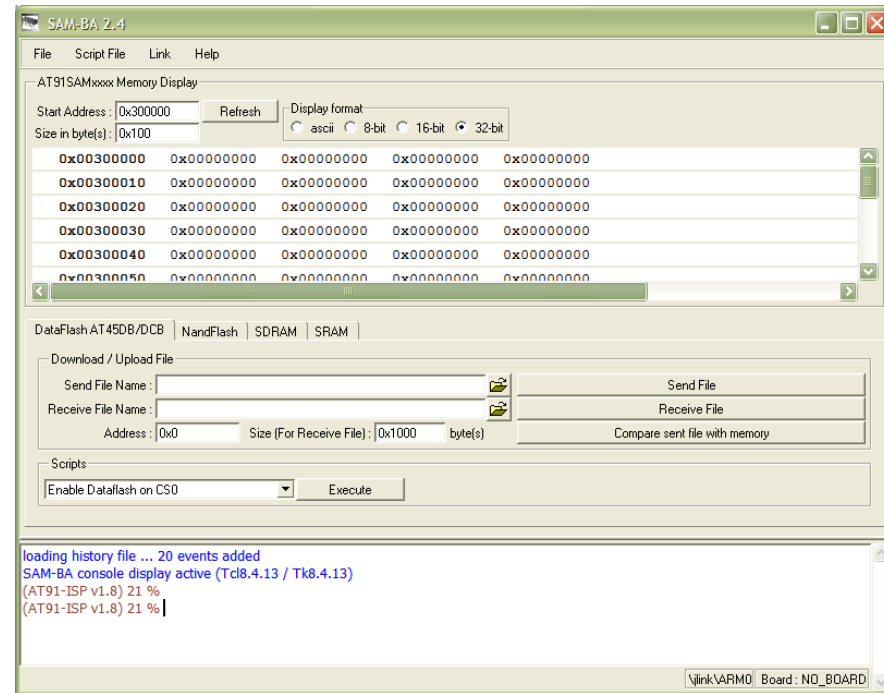
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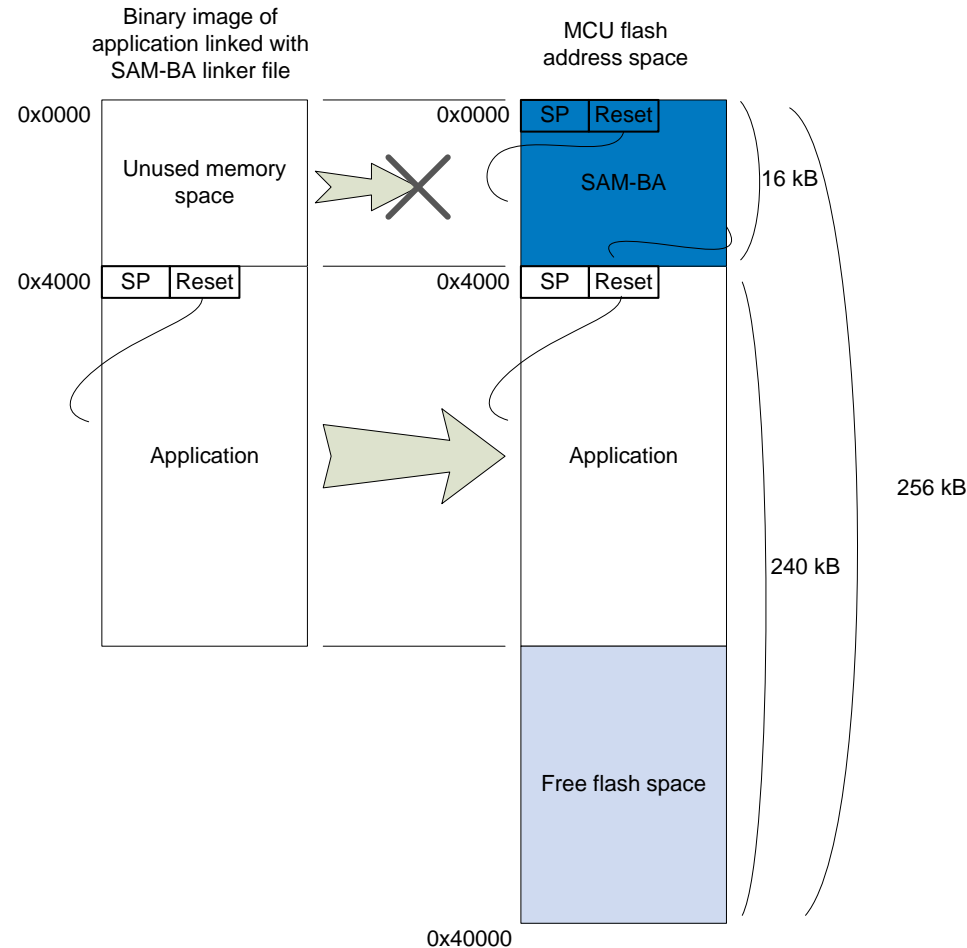
SAM-BA Support for SAM4L

- Pre-loaded in SAM4L Flash
- Compliant with SAM-BA UI
- USB CDC and UART (RS232) support
- Optional I/O pin support to force SAM-BA entry on reset using dedicated flash user page setting



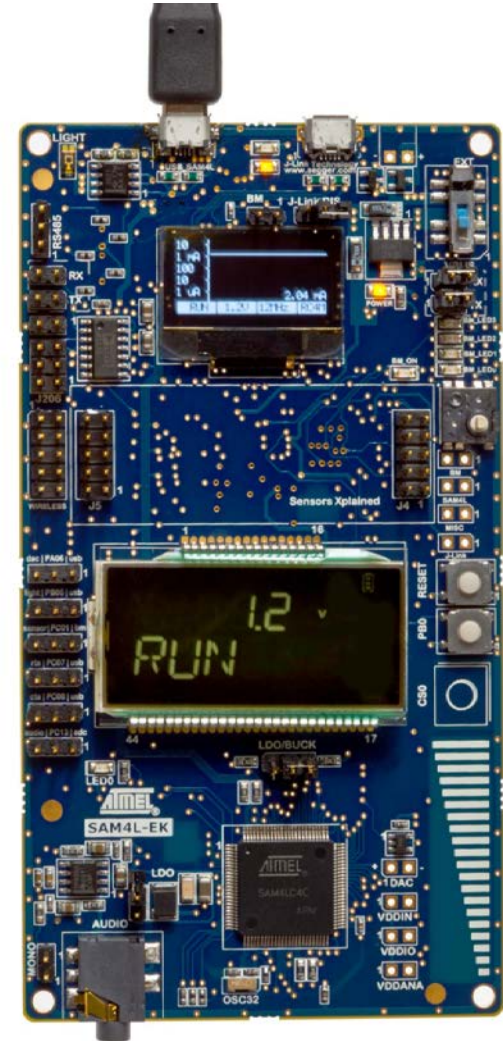
SAM-BA for SAM4L: Application Constraints

- SAM-BA is stored in Flash at 0x0.
- First region is locked (0x0 – 0x4000)
- Application must be linked and programmed at 0x4000
- SAM-BA can be erased using a JTAG/SWD debugger if not needed



SAM4L-EK: Evaluation Kit for Faster Time-to-Market

- Embedded Debugger and Programmer
- Power Measurement
 - Real-time current consumption displayed on OLED display
- LCD Display
- USB
- Capacitive Touch
- Extension Support
 - Sensor Xplained boards
 - Wireless extensions
- Atmel Studio Support





Enabling Unlimited Possibilities®

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